

EAST: 10413810 latch for sram.wsp

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- L2: (74) ((SRAM static adj3 memory static adj RAM D) near (thin\$2 adj film))
- L3: (140) inverter near4 thin adj film
- L4: (6) 2 and 3

(202) (bulk near2 (si silicon)) near9 (logic support\$4)
 (7) ((first adj2 invert?r) with (semiconductor adj2 layer)) same (second adj2 invert?r)
 (79) memory same ((low strong) adj3 invert?r) with (weak high) adj3 invert?r))
 (68185) ((ft thin adj film adj transistor) second adj semiconductor adj layer)
 (2872016) memory array cell
 (12485) ((ft thin adj film adj transistor) second adj semiconductor adj layer) near9 (m
 (6) (bulk near2 (si silicon)) near9 (logic support\$4) and (((ft thin adj film adj transist
 (1511332) memory
 (883) monolithic\$4 adj memory
 (0) (bulk near2 (si silicon)) near9 (logic support\$4) and (monolithic\$4 adj memory)
 (54634) (SRAM static adj3 memory)
 (105) (monolithic\$4 adj memory) and ((SRAM static adj3 memory D)
 (134315) (substrate bulk near2 (si silicon)) near9 (logic support\$4)
 (219) (((ft thin adj film adj transistor) second adj semiconductor adj layer) near9 (me
 (17) (((ft thin adj film adj transistor) second adj semiconductor adj layer) near9 (mer
 (330208) latch second adj (inverter inverter)
 (372114) ((SRAM static adj3 memory D) (latch second adj (inverter inverter))
 (33) (((ft thin adj film adj transistor) second adj semiconductor adj layer) near9 (mer
 (3) 10/413810

QBs: USPAT-US PGPUB; EPO; JPO; DERWENT; IBM; TDD Elevate
 Default operator: OR Highlight all hit terms initially

2 and 3

oct 2004

	D	I	I	inventor	Document#	Issue#	Title	Current	Current(X)	Revised	S	C	F	3	Image	Doc	P
1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Madurawe, R	US 2004000	20040:3	Semiconductor latches and SRAM devices	1/1			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 200400	<input type="checkbox"/>
2	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Madurawe, R	US 2004015	20040:3	Semiconductor latches and SRAM devices	438/400			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 200401	<input type="checkbox"/>
3	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Madurawe, R	US 2004000	20040:2	Semiconductor switching devices	257/347			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 200400	<input type="checkbox"/>
4	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Muragishi, T	US 5436184	19950:7	Thin film transistor and manufacturing meth	438/151	257/E21.41		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 543618	<input type="checkbox"/>
5	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Muragishi, T	US 5281828	19940:7	Thin film transistor with reduced leakage cur	257/66	257/383		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 528182	<input type="checkbox"/>
6	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	Manning, Mo	US 5214295	19930:1	Thin film field effect transistor, CMOS inver	257/67	257/389		<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	US 521429	<input type="checkbox"/>

Ready